

# 4456 Synthesizer Mirny / 4457 HF Synthesizer Mirny + Almazny

## Features

- 4-channel wide-band PLL/VCO-based microwave frequency synthesiser
- Output frequency ranges from 53 MHz to >4 GHz for 4456 Mirny only
- Up to 12 GHz with 4457 Almazny
- Higher frequency resolution than 4410/4412 Urukul
- Lower jitter, phase noise than 4410/4412 Urukul

## Applications

- Low-noise microwave source
- Quantum state control
- Driving acousto/electro-optic modulators

## General Description

The 4456 Synthesizer Mirny card is a 4hp EEM module; the 4457 HF Synthesizer Mirny + Almazny card, consisting of 4456 Mirny plus the 4-channel Almazny HF mezzanine, is a 8hp EEM module. Both Synthesizer cards add microwave generation capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

Both cards provide 4 channels of PLL frequency synthesis. 4456 Synthesizer Mirny supports output frequencies from 53 MHz to >4GHz. As 4457 HF Synthesizer with Almazny mezzanine this range is expanded up to 12 GHz.

Each channel can be attenuated from 0 to -31.5 dB by a digital attenuator. RF switches on each channel provide at least 50 dB isolation.

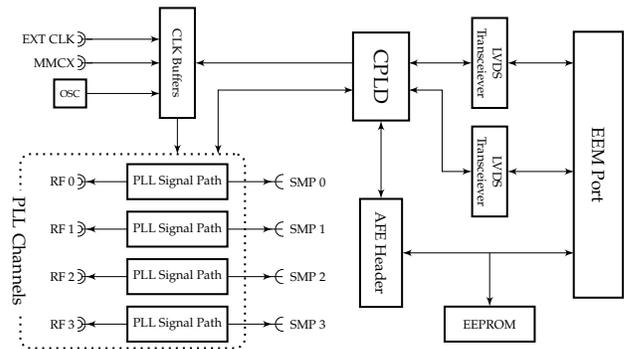


Figure 1: Simplified Block Diagram

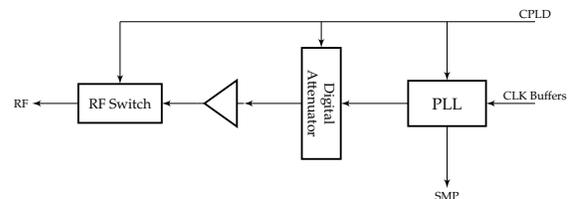


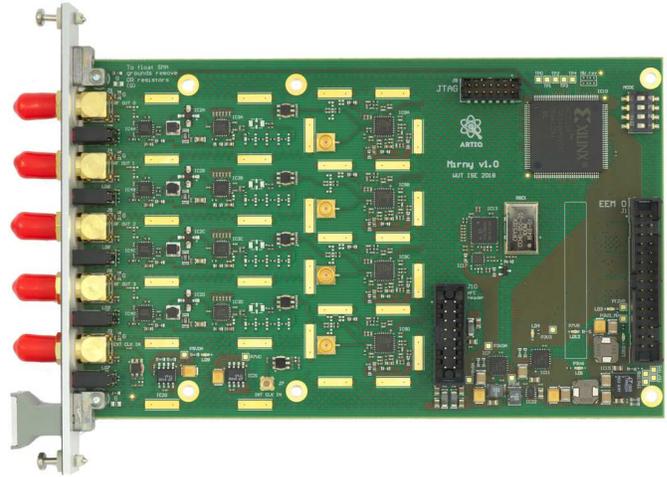
Figure 2: Simplified PLL Signal Path



Figure 3: Mirny + Almazny card



(a) Mirny and Almazny front panels



(b) Mirny, top-down view

## Source

4456 Synthesizer Mirny and the 4457 Almazny mezzanine, like all the Sinara hardware family, are open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repositories <https://github.com/sinara-hw/mirny> and <https://github.com/sinara-hw/Almazny>.

## Electrical Specifications

Specifications of parameters are based on the datasheets of the PLL IC (ADF5356<sup>1</sup>), clock buffer IC (Si53340-B-GM<sup>2</sup>), and digital attenuator IC (HMC542BLP4E<sup>3</sup>). Test results are from Krzysztof Belewicz's thesis. "Microwave synthesizer for driving ion traps in quantum computing"<sup>4</sup>.

**Table 1: Recommended Operating Conditions**

Parameter	Min.	Typ.	Max.	Unit	Conditions
Clock input Frequency <sup>1</sup>	10		250	MHz	Single-ended clock input (PLL config.)
	10		600	MHz	Differential clock input (PLL config.)
Differential input swing <sup>2</sup>	0.11		1.55	V <sub>p-p</sub>	

**Table 2: Output Specifications**

Parameter	Min.	Typ.	Max.	Unit	Conditions
Frequency	53.125		4000	MHz	4456 Mirny only
			12000	MHz	With Almazny mezzanine
Digital attenuation <sup>3</sup>	-31.5		0	dB	

<sup>1</sup><https://www.analog.com/media/en/technical-documentation/data-sheets/ADF5356.pdf>

<sup>2</sup><https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5334x-datasheet.pdf>

<sup>3</sup><https://www.analog.com/media/en/technical-documentation/data-sheets/hmc542b.pdf>

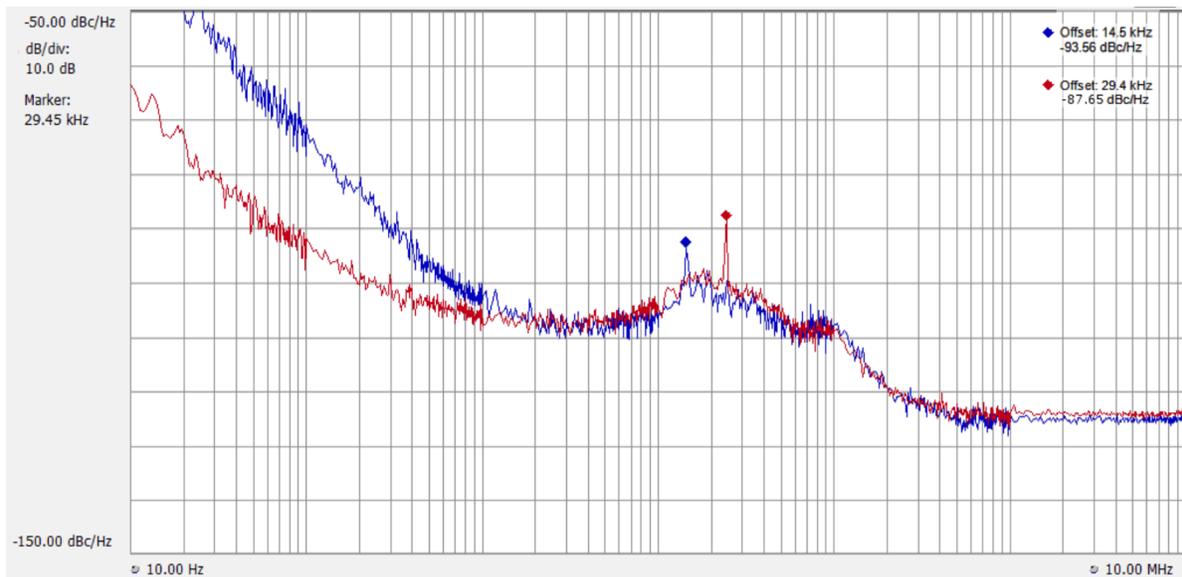
<sup>4</sup>[https://m-labs.hk/Krzysztof\\_Belewicz\\_V1.1.pdf](https://m-labs.hk/Krzysztof_Belewicz_V1.1.pdf)

**Table 3: Output Specifications, cont.**

Parameter	Min.	Typ.	Max.	Unit	Conditions
Lock time <sup>1</sup>		1.7		ms	
Resolution					
Frequency <sup>1</sup>		52		bits	
Phase offset <sup>1</sup>		24		bits	
Digital attenuation <sup>3</sup>		0.5		dB	

Phase noise performance of 4456 Mirny was tested using the ADF4351 evaluation kit<sup>4</sup>. The SPI signal was driven by the evaluation kit, converted into LVDS signal by propagating through the DIO-tester card, finally arriving at the Mirny card. 4456 Mirny was then connected to the RSA5100A spectrum analyzer for measurement.

Noise response spike can be improved by inserting an additional common-mode choke between the power supply and Mirny; note that this common-mode choke is not present on the card itself. The following is a comparison between the two setups at 1 GHz output:

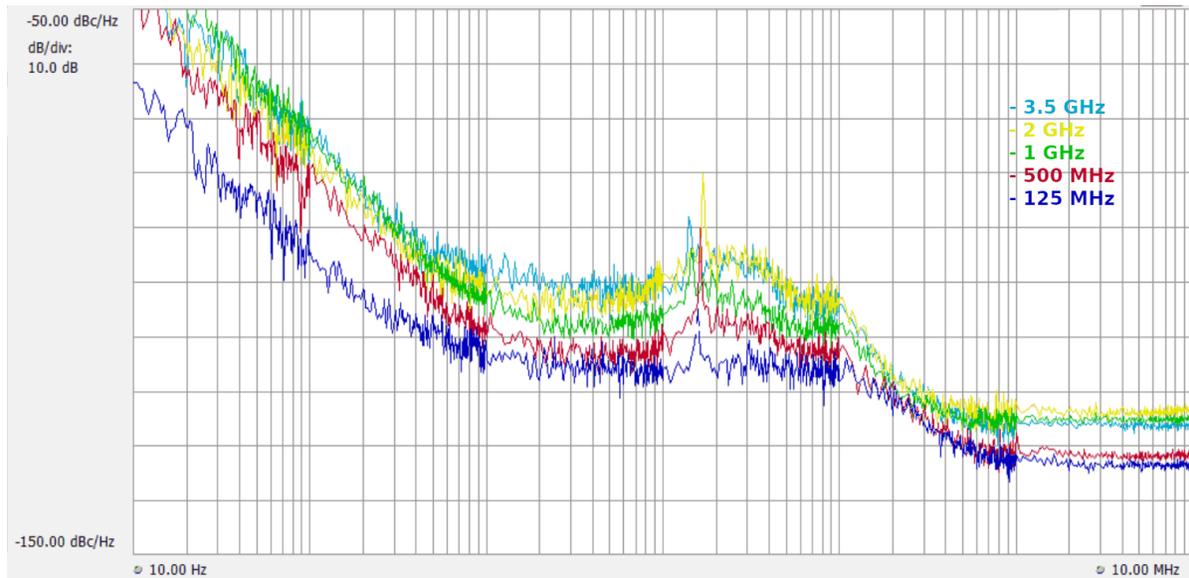
**Figure 4: Phase noise measurement at 1 GHz**

- Red: Before any modifications
- Blue: CM choke added with an 100  $\mu$ F capacitor after the CM choke

Phase noise at different output frequencies is then measured:

**Table 4: Phase noise performance**

Output frequency	Phase noise (dBc/Hz) at carrier offset				
	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
125 MHz	-114	-116	-115	-132	-133
500 MHz	-107	-129	-111	-130	-132
1 GHz	-102	-106	-107	-125	-133
2 GHz	-102	-98	-104	-123	-124
3.5 GHz	-96	-101	-103	-127	-128



**Figure 5: Phase noise measurement**

## Programmable LEDs

4456 Mirny features several status LEDs, including a two per output channel. One per channel displays RF switch status.

The 4457 Almazny mezzanine features an additional row of LEDs, one per output channel, without a fixed purpose. The associated ARTIQ module allows programming these directly through the channel set method.

## ARTIQ System Description Entry

ARTIQ/Sinara firmware/gateway is generated according to a JSON system description file, allowing gateway to be specific to and optimized for a certain system configuration.

4456 Synthesizer Mirny must be entered in the `peripherals` list of the corresponding core device in the following format:

```
{
  "type": "mirny",
  "ports": 0,
  "clk_sel": "mmc_x", // optional
  "refclk": 125e6 // optional
}
```

Replace 0 with the EEM port number used on the core device. Any port can be used. The `clk_sel` field is optional and may be specified as one of either `xo`, `mmc_x`, or `sma`. The default is `xo`. The `refclk` field is optional and the default is `100e6`.

For 4457 Mirny + Almazny, one field must be added:

```
{
  "type": "mirny",
  "almazny": true,
  "ports": 0
}
```

## Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4456 Synthesizer Mirny and 4457 Mirny + Almazny. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateway, including guides for their use, is available at <https://m-labs.hk/artiq/manual/>. Please consult the manual for details and reference material of the functions and structures used here.

### 1 GHz sinusoidal wave

Generates a 1 GHz sinusoid from RF0 with full scale amplitude, attenuated by 12 dB. Both the CPLD and the PLL channels should be initialized.

```
@kernel
def init_mirny(self):
    self.core.reset()
    self.cpld.init()
    self.pll0.init()
    self.pll0.set_frequency(1*GHz)
    self.pll0.set_att(12*dB)
    self.pll0.sw.on()
```

## Almazny paired output

Mirny and Almazny output channels are paired, and Almazny output channels output twice the frequency of the main Mirny outputs. To set Almazny HF outputs for 4457 HF Synthesizer, set the Mirny outputs to one-half the desired frequency. The above code, run with 4457 HF Synthesizer, will also output 2GHz from Almazny HF0.

## ADF5356 power control

Output power can be controlled by configuring the PLL channels individually in addition to the digital attenuators. After initialization of the PLL channel (ADF5356), the following line of code can change the output power level:

```
self.pll0.set_output_power_mu(0)
```

The parameter corresponds to a specific change of output power according to the following table<sup>1</sup>.

**Table 5: Power changes from ADF5356**

Parameter	Power
0	-4 dBm
1	-1 dBm
2	+2 dBm
3	+5 dBm

ADF5356 gives +5 dBm by default. The stored parameter in ADF5356 can be read using the following line"

```
print(self.pll0.output_power_mu())
```

## Periodic 100µs pulses

The output can be toggled on and off periodically using the RF switches. The following code emits a 100µs pulse in every millisecond. A microwave signal should be programmed in prior (such as the 1 GHz wave example).

```
while True:
    self.pll0.sw.pulse(100*us)
    delay(900*us)
```

## Ordering Information

To order, please visit <https://m-labs.hk> and choose 4456 Synthesizer Mirny or 4457 HF Synthesizer Mirny + Almazny in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to <mailto:sales@m-labs.hk>.

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